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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HENSON, MISCHITA L	

ART UNIT	PAPER NUMBER
2857	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/591,492	ACHKAR ET AL.	
	Examiner	Art Unit	
	Mi'schita' Henson	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-14 and 25-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-12* is/are allowed.

6)☒ Claim(s) *13,14 and 25* is/are rejected.

7)☒ Claim(s) *26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to the amendment field on October 15, 2008. Claims 1-7, 15-24 and 29-38 have been canceled. Claims 8-14 and 25 have been amended. Claims 8-14 and 25-26 are pending.

Claim Objections

1. Claims 10, 13 and 25 are objected to because of the following informalities:

claim 10 lines 1-2 recite "the DUT model comprises one or more of the following", Examiner suggests --the DUT model comprises at least one of the following--,

claim 13 line 18 recites "the DUT comprises one or more of:", Examiner suggests -- the DUT comprises one selected from the group consisting of:--,

claim 25 line 1 recites "A computer program product tangibly stored", Examiner suggests --A computer program product stored--.

Appropriate correction is required.

2. Claim 26 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 26 recites "A computer readable data storage medium including the computer program claimed in claim 25 stored thereon" and fails to further limit claim 25 which recites "A computer program product tangibly stored on a machine-readable medium". Thus, claim 25 includes the limitation of the computer program stored on a medium.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

1. Claim 25 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The claim is drawn to a computer program per se (specifically, claim 26 is in proper Beauregard format, therefore claim 25 is a computer program per se). Therefore, a computer program is not a physical thing (product) nor a process as they are not "acts" being performed. As such, this claim is not directed to one of the statutory categories of invention (see MPEP 2106.01), but is directed to nonstatutory functional descriptive material.

It is noted that computer programs embodied on a computer readable medium or other structure, which would permit the functionality of the program to be realized, would be directed to a product and be within a statutory category of invention, so long as the computer readable medium is not disclosed as non-statutory subject matter per se (i.e. signals or carrier waves).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lottridge et al. in US Patent 5,796,750, Brown et al. in US Publication 2005/0262399, Primeaux et al. in US Patent 6,334,121 and Childs et al. in US Patent 5,623,545.

Regarding claim 13, Lottridge et al. teaches:

A method of testing at least one embedded device under test (DUT) comprising:

determining a test configuration parameter set (a fuse map is interpreted to be a test configuration parameter, see fuse map, column 1 lines 64-65) comprising predefined DUT test sequence rules (the programming instructions are interpreted to be predefined DUT test sequence rules, see programming instructions, column 2 lines 7-11);

determining a first data set (the test vectors are interpreted to be a first data set, see test vectors, column 2 lines 7-11; see also test vectors, column 4 line 65-67) comprising input test vectors based on the test configuration parameter set;

Lottridge et al. also teaches a programming interface (column 3 lines 63-64), a compiler (column 4 lines 39-41) and a timing reference (see timing, column 6 lines 62-65). Lottridge et al. differs from the claimed invention in that it does not necessarily teach processing the first data set in a DUT model, processing the first data set and the output test vectors to determine a second data set, communicating the stabilised input test vectors to at least one DUT via a DUT independent interface, determining a third data set, comparing the third data set with the second data set to determine a comparison of actual behaviour to modelled behaviour of the at least one DUT and the DUT.

Brown et al. teaches a parsing program ([0026]) testing a behavioral model with a test vector that have been receive into the parsing program (parsing the test vector is interpreted to be processing the first data set in a DUT model, see testing a behavioral model, [0041]; matching the test vectors run in a batch with the results files that have been parsed is interpreted to be processing the first data set and the output test vectors to determine a second data set, [0051]). Childs et al. teaches using test vectors to test personal security devices (i.e. a security device, see security devices, column 2 lines 6-17; see also test vectors, Abstract and column 2 lines 6-17)

Primeaux et al. teaches pairing input and output vectors used for training (column 5 lines 10-16, column 9 lines 7-9) and comparing the resulting activation levels for the output layer (i.e. third data set, column 5 lines 10-16) with the output vector from the training data input-output vector pair (i.e. comparing the third data set with the second data set to determine a comparison of actual behaviour to modelled behaviour of the at least one DUT, column 5 lines 10-16) Primeaux et al. also teaches an interactive interface (i.e. a DUT independent interface, column 9 line 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Brown et al., Primeaux et al. and Childs et al. with Lottridge et al. because Brown et al. teaches a method of aggregating and prioritizing failures by a parsing program that helps identify failures and reduces the time required to identify and manage failures during testing ([0005]-[0006]), Primeaux et al. teaches a method for improving the integrity and security of data (column 1 lines 65-66) and Childs et al. teaches improving security functions of security

devices (column 2 lines 6-17), thereby reducing false alarms, reducing costs and improving the functionality.

3. Claims 14 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lottridge et al. in US Patent 5,796,750, Brown et al. in US Publication 2005/0262399 and Primeaux et al. in US Patent 6,334,121.

Regarding claim 14, Lottridge et al. teaches:

An apparatus adapted to test at least one embedded device (DUT), said apparatus comprising:

a processor (a programmable logic device is interpreted to be a processor, see programmable logic device, Abstract and column 1 line 62-column 2 line 5; see also microprocessor, column 3 line 57 and column 4 line 34) adapted to operate in accordance with a predetermined instruction set, a method of testing at least one embedded DUT comprising:

determining a test configuration parameter set (a fuse map is interpreted to be a test configuration parameter, see fuse map, column 1 lines 64-65) comprising predefined DUT test sequence rules (the programming instructions are interpreted to be predefined DUT test sequence, see programming instructions, column 2 lines 7-11);

determining a first data set (the test vectors are interpreted to be a first data set, see test vectors, column 2 lines 7-11; see also test vectors, column 4 line 65-67) comprising input test vectors based on the test configuration parameter set;

Lottridge et al. also teaches a programming interface (column 3 lines 63-64), a compiler (column 4 lines 39-41) and a timing reference (see timing, column 6 lines 62-65). Lottridge et al. differs from the claimed invention in that it does not necessarily teach processing the first data set in a DUT model, processing the first data set and the output test vectors to determine a second data set, communicating the stabilised input test vectors to at least one DUT via a DUT independent interface, determining a third data set and comparing the third data set with the second data set to determine a comparison of actual behaviour to modelled behaviour of the at least one DUT.

Brown et al. teaches a parsing program ([0026]) testing a behavioral model with a test vector that have been receive into the parsing program (parsing the test vector is interpreted to be processing the first data set in a DUT model, see testing a behavioral model, [0041]; matching the test vectors run in a batch with the results files that have been parsed is interpreted to be processing the first data set and the output test vectors to determine a second data set, [0051]).

Primeaux et al. teaches pairing input and output vectors used for training (column 5 lines 10-16, column 9 lines 7-9) and comparing the resulting activation levels for the output layer (i.e. third data set, column 5 lines 10-16) with the output vector from the training data input-output vector pair (i.e. comparing the third data set with the second data set to determine a comparison of actual behaviour to modelled behaviour of the at least one DUT, column 5 lines 10-16) Primeaux et al. also teaches an interactive interface (i.e. a DUT independent interface, column 9 line 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Brown et al. and Primeaux et al. with Lottridge et al. because Brown et al. teaches a method of aggregating and prioritizing failures by a parsing program that helps identify failures and reduces the time required to identify and manage failures during testing ([0005]-[0006]) and Primeaux et al. teaches a method for improving the integrity and security of data (column 1 lines 65-66), thereby reducing false alarms, reducing costs and improving the functionality.

Regarding claim 25, Lottridge et al. teaches:

A computer program product tangibly stored on a machine-readable medium, for testing at least one embedded device under test (DUT) within a data processing system, the product comprising instructions operable to cause a processor (a programmable logic device is interpreted to be a processor, see programmable logic device, Abstract and column 1 line 62-column 2 line 5; see also microprocessor, column 3 line 57 and column 4 line 34) to:

determine a test configuration parameter set (a fuse map is interpreted to be a test configuration parameter, see fuse map, column 1 lines 64-65) comprising predefined DUT test sequence rules (the programming instructions are interpreted to be predefined DUT test sequence rules, see programming instructions, column 2 lines 7-11);

determine a first data set (the test vectors are interpreted to be a first data set, , see test vectors, column 2 lines 7-11; see also test vectors, column 4 line 65-67) comprising input test vectors based on the test configuration parameter set;

Lottridge et al. also teaches a programming interface (column 3 lines 63-64), a compiler (column 4 lines 39-41) and a timing reference (see timing, column 6 lines 62-65). Lottridge et al. differs from the claimed invention in that it does not necessarily teach process the first data set in a DUT model, process the first data set and the output test vectors to determine a second data set, communicate the stabilised input test vectors to at least one DUT via a DUT independent interface, determine a third data set and compare the third data set with the second data set to determine a comparison of actual behaviour to modelled behaviour of the at least one DUT.

Brown et al. teaches a parsing program ([0026]) testing a behavioral model with a test vector that have been receive into the parsing program (parsing the test vector is interpreted to be process the first data set in a DUT model, see testing a behavioral model, [0041]; matching the test vectors run in a batch with the results files that have been parsed is interpreted to be process the first data set and the output test vectors to determine a second data set, [0051]).

Primeaux et al. teaches pairing input and output vectors used for training (column 5 lines 10-16, column 9 lines 7-9) and comparing the resulting activation levels for the output layer (i.e. third data set, column 5 lines 10-16) with the output vector from the training data input-output vector pair (i.e. compare the third data set with the second data set to determine a comparison of actual behaviour to modelled behaviour of the at least one DUT, column 5 lines 10-16) Primeaux et al. also teaches an interactive interface (i.e. a DUT independent interface, column 9 line 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Brown et al. and Primeaux et al. with Lottridge et al. because Brown et al. teaches a method of aggregating and prioritizing failures by a parsing program that helps identify failures and reduces the time required to identify and manage failures during testing ([0005]-[0006]) and Primeaux et al. teaches a method for improving the integrity and security of data (column 1 lines 65-66), thereby reducing false alarms, reducing costs and improving the functionality.

Allowable Subject Matter

4. Claims 8-12 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter:

Claim 8 is allowed because the closest prior art, Ricchetti et al. in WO 03/048794 in US Patent 5,424,633 and Oke et al. in US Patent 5,642,057, fail to anticipate or render obvious a method of testing at least one embedded device under test (DUT) comprising:

wherein the predefined timing reference is derived from a logical connection port adapted to indicate a predefined timing reference for determining a point in time at which to sample an output vector as the corresponding output vector in an input/output vector pair, **in combination** with all other limitations in the claim as defined by the applicant.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mi'schita' Henson whose telephone number is (571) 270-3944. The examiner can normally be reached on Monday - Thursday 7:30 a.m. - 4:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on (571) 272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

12/11/08
/Mi'schita' Henson/
Examiner, Art Unit 2857

/Eliseo Ramos-Feliciano/
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